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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/477,099	01/04/2000	FREDERICK S. DUNLAP	P04056	8711

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EXAMINER	
BETIT, JACOB F	

ART UNIT	PAPER NUMBER
2175	9

DATE MAILED: 02/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/477,099	DUNLAP ET AL.	
	Examiner	Art Unit	
	Jacob F. Betit	2175	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/19/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

SAM RIMELL
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "106", "120", and "300" have all been used to designate an SRAM cell in figure 2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The arrangement of the disclosed application does not conform with 37 CFR 1.77(b).

The section headings are boldfaced throughout the disclosed specification. Section headings should not be underlined and/or **boldfaced**. Appropriate corrections are required according to the guidelines provided below:

3. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9, 11-19, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumura et al. (U.S. patent No. 5,365,475).

As to claim 1, Matsumura et al. teaches a static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line (see figure 3, BL and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program (see figure 3, G_1, G_2, V_1, and V_2).

As to claim 11, Matsumura et al. teaches a data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU (see figure 15), said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing bits of said boot-up program (see column 1, lines 15-19), each of said storage cells comprising:

a data latch having an input and an output (see figure 3, BL and $\overline{BL}$), said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line (see figure 3, NA); and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line (see figure 3, NB); and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device (see figure 3, G_1, G_2, V_1, and V_2).

As to claims 2 and 12, Matsumura et al. teaches wherein said biasing circuit initially applies power only to said first inverter (see column 7, line 62 through column 8, line 36).

As to claims 3 and 13, Matsumura et al. teaches wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state (see column 7, line 62 through column 8, line 36).

As to claims 4 and 14, Matsumura et al. teaches wherein said biasing circuit subsequently applies power to said second inverter (see column 9, lines 8-14).

As to claims 5 and 15, Matsumura et al. teaches wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state (see column 9, lines 8-14).

As to claims 6 and 16, Matsumura et al. teaches wherein said biasing circuit initially applies power only to said second inverter (see column 7, line 62 through column 8, line 36).

As to claims 7 and 17, Matsumura et al. teaches wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state (see column 7, line 62 through column 8, line 36).

As to claims 8 and 18, Matsumura et al. teaches wherein said biasing circuit subsequently applies power to said first inverter (see column 9, lines 8-14).

As to claims 9 and 19, Matsumura et al. teaches wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state (see column 9, lines 8-14).

As to claim 21, Matsumura et al. teaches a method for use in a storage cell in a static random access memory (SRAM) device (see column 1, lines 15-19), the storage cell having an input and an output and comprising 1) a first inverter having an input

coupled to the storage cell input and an output coupled to the storage cell output (see figure 3, NA) and 2) a second inverter having an input coupled to the storage cell output and an output coupled to the storage cell input (see figure 3, NA), a method of forcing the storage cell output to a known logic state when power is applied to the SRAM device (see abstract) comprising the step of:

initially applying power only to one of the first inverter and the second inverter, wherein the initial application of power only to one of the first inverter and the second inverter forces a selected one of the first inverter output and the second inverter output to a Logic 1 state (see column 7, line 62 through column 8, line 36).

As to claims 22, Matsumura et al. teaches including the further step of subsequently applying power to the initially unpowered one of the first inverter and the second inverter, wherein the subsequent application of power to the initially unpowered one of the first inverter and the second inverter forces the output of the unselected one of the first inverter output and the second inverter output to a Logic 0 state (see column 9, lines 8-14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al. (U.S. patent No. 5,365,475) in view of Shimazu et al. (U.S. patent No. 4,777,623).

As to claims 10 and 20, Matsumura et al. does not teach wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state.

Shimazu et al. teaches wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state (see column 3, line 65 through column 4, line 14).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. to include said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device,

thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. by the teachings of Shimazu et al. because said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second 1/O line to said known logic state would allow the device to be set or reset (see Shimazu et al., column 1, lines 7-10).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Japanese patent No. 06-060667 to Teruo et al. for teaching a semiconductor memory device that initializes data memory right after power input and allows usual access after the initialization is over.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob F. Betit whose telephone number is (703) 305-3735. The examiner can normally be reached on Monday through Friday 9 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (703) 305-3830. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jfb
February 18, 2004

SAM RIMELL
PRIMARY EXAMINER